Listing of Claims:

1. (Cancelled)

2.-6. (Cancelled)

7.- 21. (Cancelled)

22. (Currently amended) A switch element, comprising:

an input routing portion including a switch matrix input port for receiving data;

a buffer portion including a plurality of buffers;

a switch matrix portion for routing data out from the plurality of buffers;

an output arbitrating portion, including,

a plurality of schedulers for receiving the data from the plurality of buffers through the switch matrix,

a selector for receiving data from the plurality of schedulers, the selector enabling output from the switch element through a switch matrix output port;

an additional input routing portion including an additional switch matrix input port for receiving data;

an additional buffer portion including an additional plurality of buffers, the switch matrix portion routing data out from the additional plurality of buffers;

an additional output arbitrating portion, including an additional plurality of schedulers for receiving the data from the additional plurality of buffers through the additional switch matrix, and

an additional selector for receiving data from the additional plurality of schedulers, the additional selector enabling output from the switch element through an additional switch matrix output port;

wherein the output arbitrating portion receives data from the buffer portion and the additional buffer portion through the switch matrix portion and the additional switch matrix portion.

25. (Currently Amended) The switch element as recited in claim 22 [[24]], wherein the additional output arbitrating portion receives data from the buffer portion and the additional buffer portion through the switch matrix portion and the additional switch matrix portion.

26. (Previously presented) The switch element as recited in claim 22, wherein the input routing portion receives data from a plurality of traffic generators.

27. (Currently Amended) The switch element as recited in claim 22 [[23]], wherein a plurality of traffic acceptors receive data from an output arbitrating structure.

28. (Previously presented) A switch element, comprising:

a first input routing portion including a first switch matrix input port for receiving data;

a first buffer portion including a first plurality of buffers;

a switch matrix portion for routing data out from the first plurality of buffers and a second plurality of buffers;

a first output arbitrating portion, including,

a first plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix,

a first selector for receiving data from the first plurality of schedulers, the first selector enabling output from the switch element through a first switch matrix output port;

a second input routing portion including a second switch matrix input port for receiving data;

a second buffer portion including the second plurality of buffers;

a second output arbitrating portion, including,

a second plurality of schedulers for receiving the data from the first plurality of buffers and the second plurality of buffers through the switch matrix,

a second selector for receiving data from the second plurality of schedulers, the second selector enabling output from the switch element through a second switch matrix output port;

a plurality of traffic generators for inputting data into the first input routing portion and the second input routing portion; and

a plurality of traffic acceptors to receive data from the first output arbitrating portion and the second output arbitrating portion.